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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,781	08/28/2003	Phillip E. Byrd	M4065.0468/P468-B	5845
24998	7590	09/12/2006	EXAMINER	
DICKSTEIN SHAPIRO LLP 1825 EYE STREET NW Washington, DC 20006-5403			ISAAC, STANETTA D	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 10/649,781	Applicant(s) BYRD ET AL	
	Examiner Stanetta D. Isaac	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 37-52 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 37-52 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>8/28/03</u> . | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

This Office Action is in response to the application filed on 8/28/03. Currently, claims 37-52 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 8/28/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 37-52 are rejected under 35 U.S.C. 102(e) as being anticipated by Fenner et al.,
US Patent 6,548,826.

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Fenner discloses the semiconductor method as claimed. See figures 1-6, and corresponding text, where Fenner teaches, pertaining to claim 37, a method of testing a plurality of dies fabricated on a wafer, said method comprising: connecting a first terminal **106** of each of said plurality of dies **200** to a common signal conductor **202, 204, 208** through respective temporary isolation devices **210** which allow said dies to receive a signal from said common signal conductor during a first test procedure (figures 4 and 5; col. 6, lines 55-67; col. 7, lines 1-4 and 29-40, a full test of the dies are performed as a first test); and connecting said first terminal **106** of at least some of said plurality of dies **200** to another conductor during a second test procedure, said temporary isolation devices **210** being activated during said second test procedure to isolate said first terminal of said at least some of said dies from said common signal conductor **202, 204, 208** during said second test procedure (figures 4 and 5; col. 7, lines 29-44, additional test are performed for the dies that past the first test).

Fenner teaches, pertaining to claim 38, a method of testing a semiconductor die on a wafer comprising: (1) applying voltage **500** to a first voltage line **202, 204, 208** which connects with a plurality of dies **200** on said wafer through respective temporary isolation devices **210** (figures 4 and 5; col. 6, lines 55-67; col. 7, lines 1-26) (2) removing voltage from said first voltage line (col. 7, lines 27-35, *Note*: the Examiner takes the position that the after the disconnection of the power supply, the dies of electrically isolated by the implied temporary isolation devices); and (3) applying voltage to a die by connecting a probe to a first voltage terminal associated with said die, said die being isolated from said first voltage line by a respective temporary isolation device (col. 7, lines 33-35, *Note*: the Examiner takes the position that a probe is included in the post burn-in inspection procedure).

Fenner teaches, pertaining to claim 39, wherein steps (1) and (2) are performed before step (3) (col. 7, lines 10-27 and 29-35).

Fenner teaches, pertaining to claim 40, further comprising permanently isolating a die from said common first voltage conductor as a result of tests performed in said first and second test procedures (figure 5; col. 6, lines 19-23 and lines 35-40).

Fenner teaches, pertaining to claim 41, wherein step (1) is performed after steps (2) and (3) (col. 6, lines 20-30).

Fenner teaches, pertaining to claim 42, further comprising permanently isolating one or more of said plurality of dies found defective during at least said first or second test procedure from said common conductor (col. 7, lines 45-47).

Fenner teaches, pertaining to claim 43, wherein said permanently isolating one or more of said plurality of dies comprises activating a permanent isolation device coupled between said between said common conductor and one or more of said plurality of dies found defective during said first or second test procedure (col. 6, lines 20-30).

Fenner teaches, pertaining to claim 44, wherein said permanent isolation device comprises a laser activated fuse (col. 6, lines 20-30).

Fenner teaches, pertaining to claim 45, a method of testing a semiconductor wafer comprising: supplying first signal **500** to a first signal line **202, 204, 208** on a semiconductor wafer coupled to a plurality of dies **200** fabricated on said wafer during a first test mode, each die comprising an integrated circuit and a first terminal **106** used to apply said first signal to internal components of said die (figures 4 and 5; col. 6, lines 55-67; col. 7, lines 1-26); determining one or more dies to temporary isolate from said plurality of dies (col. 7, lines 27-35, *Note*: the

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Examiner takes the position that the after the disconnection of the power supply, the dies of electrically isolated by the temporary devices); supplying a second signal to a unidirectional circuit device on said one or more dies to temporarily isolate from said plurality of dies during a second test mode (col. 7, lines 27-35, *Note*: the Examiner takes the position that the after the disconnection of the power supply, the dies of electrically isolated by the implied temporary isolation devices); and temporarily isolating said one or more dies from said plurality of dies when said second signal is supplied to said unidirectional circuit device (col. 7, lines 27-35); wherein, each unidirectional circuit device is coupled between said first signal line **202, 204, 208** and said first terminal **106** of a respective die for allowing said first signal to move in only one direction between said first signal line and the first terminal of a respective die (figures 4 and 5; col. 7, lines 29-35).

Fenner teaches, pertaining to claim 46, wherein said supplying a second signal to said one or more dies to temporarily isolate said one or more dies from said plurality of dies comprises supplying said second signal to one of a plurality of first and second conductive surfaces, one of said plurality of first conductive surfaces being coupled between an input of each said plurality of unidirectional circuit devices and said first signal line, one of said plurality of second conductive surfaces being coupled between an input each said plurality of unidirectional circuit devices and said first terminal of a respective die (figures 4 and 5; col. 5, lines 35-51).

Fenner teaches, pertaining to claim 47, wherein said temporarily isolating said one or more dies from said plurality of dies comprises selectively decoupling one of said plurality of dies that said unidirectional circuit device is coupled from said first signal line when at least said

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second signal is applied to a conductive probe pad coupled between said unidirectional circuit device and said first terminal (figure 5; col. 5, lines 52-56).

Fenner teaches, pertaining to claim 48, further comprising selectively supplying a third signal to a second terminal coupled between said unidirectional circuit device and said first signal line, said supplying a second signal to a unidirectional circuit device on said one or more dies to temporarily isolate from said plurality of dies comprises supplying said second signal to a third terminal coupled between said unidirectional circuit device and said first terminal, said second and third terminals receiving a respective second and third signal in a first test mode (figure 5; col. 7, lines 10-40).

Fenner teaches, pertaining to claim 49, wherein the unidirectional circuit device comprises a diode, said first test mode reverse biases said diode to electrically decouple said first signal conductor with said circuitry for performing an electrical function on one of said dies (col. 5, lines 44-51).

Fenner teaches, pertaining to claim 50, further comprising permanently isolating one or more of said plurality of dies found defective during said first or second test modes from said first signal line (col. 6, lines 20-30).

Fenner teaches, pertaining to claim 51, wherein said permanently isolating one or more of said plurality of dies comprises activating a permanent isolation device coupled between said first signal line and one or more of said plurality of dies found defective during said first or second test modes (col. 6, lines 20-30).

Fenner teaches, pertaining to claim 52, wherein said permanent isolation device comprises a laser activated fuse (col. 6, lines 20-30).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
September 3, 2006



MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER